CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) An insulated gate transistor for conduction using charge carriers of a predetermined conductivity type, comprising:

a semiconductor body layer;

a source electrode extending across a source region of the semiconductor body layer defining a Schottky potential barrier between the source electrode and the source region of the semiconductor body layer,

a drain electrode connected to the semiconductor body layer; and

a gate electrode for controlling transport of carriers of the predetermined carrier type from the source electrode to the source region of the semiconductor body layer across the barrier when the source region is depleted;

wherein the gate electrode **and source electrode are** ~~is~~ arranged in [[an]] **a wholly opposed laterally** overlapping relationship to each other, the source electrode **and gate electrode being centrally located above the semiconductor body; and**

wherein the gate electrode is located on the opposite side of the semiconductor body layer to the source electrode having a gate insulator layer between the gate electrode and the semiconductor body layer; ~~and~~

wherein the gate electrode is spaced from the source electrode by at least the combined full thickness of the semiconductor body layer and the gate insulator over the whole of the gate-controlled region of the Schottky barrier.

2. (Currently Amended) An insulated gate transistor for conduction using the charge carriers of a predetermined conductivity type, comprising:

a semiconductor body layer having a thickness of at least 10 nm;

a source electrode extending across a source region of the semiconductor body layer defining a potential barrier between the source electrode and a source region of the semiconductor body layer,

a drain electrode connected to the semiconductor body layer; and

a gate electrode for controlling transport of carriers of the predetermined carrier type from the source electrode to the source region of the semiconductor body layer across the barrier when the source region is depleted;

wherein the gate electrode **and source electrode are** ~~is~~ arranged in [[an]] **a wholly opposed laterally** overlapping relationship to each other, the source electrode **and gate electrode being centrally located above the semiconductor body; and**

wherein the gate electrode is located on the opposite side of the semiconductor body layer to the source electrode having a gate insulator layer between the gate electrode and the semiconductor body layer; and

wherein the gate electrode is spaced from the source electrode by at least the combined thickness of the full thickness of the semiconductor body layer and the gate insulator over the whole of the gate-controlled region of the source barrier.

3. (Previously Presented) A transistor according to claim 1 including dopant impurities in the semiconductor body layer under the source electrode for controlling the effective barrier height.

4. (Original) A transistor according to claim 3 wherein the dopant is a shallow implant of donor impurities to raise the effective barrier height to holes and to lower the effective barrier height to electrons.

5. (Currently Amended) A transistor according to ~~any preceding~~ claim 1 further comprising a field relief structure at the lateral edge of the source electrode facing the drain electrode.

6. (Previously Presented) A transistor according to claim 5 wherein the drain electrode is connected to a drain region of the semiconductor body layer, the drain region being spaced from the source region by an intermediate region of the semiconductor body

layer, and the field relief structure is the intermediate region of the semiconductor body layer between the source region and the drain region, the intermediate region being compensated.

7. (Previously Presented) A transistor according to claim 5 wherein the drain electrode is connected to a drain region of the semiconductor body layer, the drain region being spaced from the source region by an intermediate region of the semiconductor body layer, and the field relief structure comprises an extension to the source electrode extending laterally across at least part of the intermediate region, separated from the said part of the intermediate region by a field relief insulating layer.

8. (Currently Amended) A transistor according to **claim 1** ~~any preceding claim~~ wherein the drain electrode is connected to a drain region of the semiconductor body layer, the drain region being spaced from the source region by an intermediate region of the semiconductor body layer, and the lateral extent of the intermediate region between the drain region and the source region is less than 5 micrometer.

9. (Previously Presented) A transistor according to claim 1 wherein the lateral extent of the gate electrode towards the drain is overlapped wholly by the source electrode.

10. (Previously Presented) A transistor according to claim 1 comprising a pair of

drain electrodes and corresponding drain regions of the semiconductor body layer laterally on either side of the source region.

11. (Previously Presented) A transistor according to claim 1 wherein the potential barrier has a barrier potential for the predetermined charge carrier type of between 0.25 times and 0.75 times the band gap of the semiconductor of the semiconductor body layer.

12. (Previously Presented) A transistor according to claim 2 further comprising a heterojunction layer between the source electrode and the semiconductor body layer forming the barrier.

13. (Previously Presented) A transistor according to claim 1 wherein the semiconductor body layer is a thin film of deposited semiconductor material.

14. (Previously Presented) A transistor according to claim 1 wherein the semiconductor body layer is of amorphous silicon.

15. (Previously Presented) A transistor according to claim 1 wherein the semiconductor body layer is of polysilicon.

16. (Previously Presented) A transistor according to claim 1 wherein the

semiconductor body layer is of organic semiconductor.

17. (Currently Amended) An insulated gate transistor for conduction using charge carriers of a predetermined conductivity type, comprising:

a semiconductor body layer;

a laterally-extending source electrode defining a lateral barrier at one major side of the semiconductor body layer;

a drain electrode laterally spaced along the semiconductor body layer from the source electrode by an intermediate region of the semiconductor body layer;

wherein the gate electrode and source electrode are arranged in a wholly opposed laterally overlapping relationship to each other, the source electrode and gate electrode being centrally located above the semiconductor body; and

[[a]] **wherein the** gate electrode **extends** [[extending]] laterally on the opposite major side of the semiconductor body layer to the source electrode to define a gate-controlled region of the semiconductor body layer extending across the semiconductor body layer to the source barrier;

a gate insulator layer between the gate electrode and the semiconductor body layer; and

a field relief structure on the edge of the source region facing the drain region.

18. (Currently Amended) An insulated-gate transistor for conduction using charge

carriers of a predetermined conductivity type, comprising:

a semiconductor layer that provides a body portion of the transistor between a source of the said carriers and a drain for the said carriers; and

an insulated gate including a gate electrode coupled to the body portion via an intermediate gate-dielectric layer;

wherein the source comprises a barrier to the said carriers between a source electrode and the semiconductor layer so as to inhibit carrier flow from the source into the body portion except as controlled by the insulated gate;

the source and the insulated gate are located at respective opposite major sides of the semiconductor layer in [[an]] **a wholly** opposed laterally-overlapping relationship which separates the source from the insulated gate by at least an intermediate thickness of the semiconductor layer**, and wherein the source electrode and insulated gate are centrally located above the semiconductor body**;

and the laterally-overlapping insulated gate is coupled to the source barrier via the intermediate thickness of the semiconductor layer so as to permit transistor conduction by controlled emission of said carriers across the source barrier by voltage applied between the gate and source electrodes upon depletion of the body portion across the intermediate thickness of the semiconductor layer from the insulated gate.

19. (Currently Amended) A transistor comprising a source electrode **on one side of a semiconductor body layer and a gate electrode in a wholly opposed laterally-overlapping relationship to the source electrode** on the opposite side of a semiconductor body layer ~~to an insulated gate electrode~~, **and wherein the source electrode and insulated gate are centrally located above the semiconductor body**;
and a drain electrode connected to the semiconductor body layer, wherein the source electrode has a potential barrier to the semiconductor body layer, and source-drain current is controlled by the gate voltage upon depletion of a region of the semiconductor body layer adjacent to the source barrier by the application of suitable source-drain voltage and gate voltage.

20. (Currently Amended) **A method of using the** ~~Use of a~~ transistor according to claim 1, including applying a voltage between the source, gate and drain electrode to substantially deplete the whole of the source region of the semiconductor body layer in the region of the gate electrode and to cause carriers of the predetermined conductivity type to be emitted by the source electrode across the barrier and across the depleted source region to the drain region and then to the drain electrode.

21. (Currently Amended) **A method of using the** ~~Use of a~~ transistor according to ~~any~~ claim 20 including **further** varying the source-gate voltage to vary the source-drain current.

22. (Previously Presented) A transistor arrangement, comprising a substrate; and a plurality of transistors according to claim 1 distributed over the substrate.

23. (Currently Amended) A transistor arrangement according to claim 22 including both n-type and p-type transistors ~~according to claim 1~~.

24. (Original) A transistor arrangement according to claim 23 wherein there is a shallow implant of donor impurities under the barriers of p-type and n-type transistors to raise the effective barrier height to holes in the p-type transistors and to lower the effective barrier height to electrons in the n-type transistors.

25. (Currently Amended) A transistor circuit, including an insulated gate field effect transistor having a semiconductor body layer, a source electrode and a gate electrode arranged in **an opposed wholly laterally overlapping relationship** ~~opposed relationship~~ on opposite sides of the semiconductor body layer, with a barrier between the source electrode and the semiconductor body layer and a gate insulator between the semiconductor body layer and the gate, and a drain electrode connected to the semiconductor body layer; and

a circuit arranged to apply voltages to source, gate and drain electrodes to deplete the semiconductor body layer in the region of the source electrode and to control the barrier height of the barrier by the source-gate voltage to control the emission of carriers from the source electrode to the semiconductor body layer and hence to control the source-

drain current by the source-gate voltage.

26. (Previously Presented) A method of operating a transistor having a source electrode, a drain electrode, a semiconductor body layer having a source region in contact with the source electrode and a drain region in contact with the drain electrode, and an insulated gate opposed to the source electrode, the method including:

applying a voltage between the source, gate and drain to substantially deplete the whole of the source region of the semiconductor body layer and to cause carriers to be emitted by the source electrode across the barrier and across the depleted source region to the drain region and then to the drain electrode.

27. (Original) A method according to claim 26 including holding the source-drain voltage at a value that depletes the source region and varying the source-gate voltage to control the current flowing from source to drain.